AMENDMENTS TO THE CLAIMS

Please cancel claims 1-15 without prejudice. All pending claims are listed below:

16. (New) An apparatus, comprising:

at least two processors, each processor including a plurality of pipeline stages for processing at least some of the same instructions;

wherein each pipeline stage includes a parity bit generator to generate at least one parity bit for each pipeline stage; and

a comparing circuit to compare the parity bit of a stage of one of the at least two processors to the parity bit of the same stage of another of the at least two processors, and indicate an error when the parity bits are different in value.

17. (New) The apparatus of claim 16, wherein the comparing circuit causes both processors to flush and restart when the parity bits are different in value.

18. (New) The apparatus of claim 16, wherein the comparing circuit indicates an error before an answer is computed by both processors at the completion of the plurality of pipelined stages for both processors.

19. (New) The apparatus of claim 16, wherein the comparing circuit indicates an error in response to a single event upset occurring in at least one processor.

20. (New) The apparatus of claim 16, wherein the comparing circuit indicates an error in response to single bit and double bit errors occurring in the system.

21. (New) A machine-readable medium having stored thereon a plurality of executable instructions, the plurality of instructions comprising instructions to:

process at least some of the same instructions for at least two processors;

compare at least one parity bit of a first pipeline stage for one processor with at least one parity bit of a second pipeline stage of another processor performing a similar function as the pipeline stage; and

indicate an error when the parity bits are different in value.

22. (New) The medium of claim 21, wherein said instructions include instructions to flush and restart both processors when the parity bits are different in value.

23. (New) The medium of claim 21, wherein said instructions include instructions to indicate an error before an answer is computed by both processors at the completion of the plurality of pipelined stages for both processors.

24. (New) The medium of claim 21, wherein the difference in parity bit value is caused by a single event upset occurring in at least one processor.

25. (New) The medium of claim 21, wherein said instructions include instructions to indicate an error in response to both single bit and double bit errors occurring in at least one processor.

26. (New) A system comprising:

a memory storing a plurality of instructions;

at least two processors, each processor coupled to said memory and including a

plurality of pipeline stages for processing at least some of the same instructions from said memory;

wherein each pipeline stage includes a parity bit generator to generate at least one parity bit for each pipeline stage; and

a comparing circuit to compare the parity bit of a stage of one of the at least two processors to the parity bit of the same stage of another of the at least two processors, and indicate an error when the parity bits are different in value.

27. (New) The system of claim 26, wherein the comparing circuit causes both processors to flush and restart when the parity bits are different in value.

28. (New) The system of claim 26, wherein the comparing circuit indicates an error before an answer is computed by both processors at the completion of the plurality of pipelined stages for both processors.

29. (New) The system of claim 26, wherein the comparing circuit indicates an error in response to a single event upset occurring in at least one processor.

30. (New) The system of claim 26, wherein the comparing circuit indicates an error in response to single bit and double bit errors occurring in the system.